CLAIMS

1. A method of making a semiconductor structure, comprising:

determining a first polish time, sufficient to planarize a layer on a semiconductor substrate;

polishing the layer for said first polish time, to planarize the layer; and

polishing the layer to a predetermined thickness.

2. The method of claim 1, further comprising, prior to the determining of said first polish time, measuring the thickness of the layer.

3. The method of claim 1, further comprising, prior to the determining of said first polish time, measuring the pattern density of the layer.

4. The method of claim 1, further comprising, prior to the determining of said first polish time, identifying the composition of the layer.

5. The method of claim 1, further comprising determining a second polish time sufficient to reduce the thickness of the layer after planarization to the predetermined thickness;

wherein the polishing of the layer to the predetermined thickness comprises polishing the layer for said second polish time.

6. A process for making a plurality of semiconductor structures, comprising:

making each semiconductor structure by the method of claim 1;

wherein the Cpk of the process is at least 1.

7. A process for making a plurality of semiconductor structures, comprising:

making each semiconductor structure by the method of claim 5;

wherein the Cpk of the process is at least 1.

8. The process of claim 7, wherein the making each semiconductor comprises, prior to the determining of said first polish time, measuring the thickness of the layer, the pattern density of the layer, and identifying the composition of the layer.

9. A method of making a semiconductor structure, comprising:

determining a polish time sufficient to reduce the thickness of a layer on a semiconductor substrate to a predetermined thickness;

polishing the layer such that the layer becomes planar; and

polishing the layer for said polish time to reduce the thickness of the layer after planarization to the predetermined thickness.

10. The method of claim 9, further comprising, prior to the determining of said polish time, measuring the polish rate of a blanket wafer.

11. A process for making a plurality of semiconductor structures, comprising:

making each semiconductor structure by the method of claim 9; wherein the Cpk of the process is at least 1.

12. In a method of making a semiconductor structure, including polishing a layer by chemical mechanical polishing, the improvement comprising determining a first polish time sufficient to make the layer planar; determining a second polish time to reduce the thickness of the planar layer; and polishing for a third polish time equal to the sum of the first and second polish times.

13. A method of making a semiconductor device, comprising:

making a semiconductor structure by the method of claim 1; and

forming a semiconductor device from said structure.

14. A method of making an electronic device, comprising:

making a semiconductor device by the method of claim 13; and

forming an electronic device, comprising said semiconductor device.

15. A method of making a semiconductor device, comprising:
making a semiconductor structure by the method of claim 5; and
forming a semiconductor device from said structure.

16. A method of making an electronic device, comprising:
making a semiconductor device by the method of claim 15; and
forming an electronic device, comprising said semiconductor device.

17. A method of making a semiconductor device, comprising:
making a semiconductor structure by the method of claim 9; and
forming a semiconductor device from said structure.

18. A method of making an electronic device, comprising:
making a semiconductor device by the method of claim 17; and
forming an electronic device, comprising said semiconductor device.

19. A machine readable medium, comprising:
code, imbedded in the machine readable medium, for determining a first polish time, sufficient to planarize a layer on a semiconductor substrate.

20. The machine readable medium of claim 19, further comprising:
code, imbedded in the machine readable medium, for determining a second polish time, sufficient to reduce the thickness of the layer after planarization to a predetermined thickness.

21. The machine readable medium of claim 20, further comprising:
code, imbedded in the machine readable medium, for driving a chemical mechanical polishing apparatus for the sum of said first and second polishing times.

22. The machine readable medium of claim 20, wherein

said code for determining a first polish time comprises means for determining a first polish time; and

said code for determining a second polish time comprises means for determining a second polish time.

23. A system for making a semiconductor structure, comprising:

a chemical mechanical polishing apparatus; and

the machine readable medium of claim 19.

24. A method of making a semiconductor structure, comprising:

polishing a layer on a semiconductor substrate with the system of claim 23.

25. A method of making a semiconductor device, comprising:

making a semiconductor structure by the method of claim 24; and

forming a semiconductor device from said structure.

26. A method of making an electronic device, comprising:

making a semiconductor device by the method of claim 25; and

forming an electronic device, comprising said semiconductor device.